Electronic Version
Stylesheet Version v1.1.1

Description

A Divide-by-X.5 Circuit with Frequency Doubler and Differential Oscillator

BACKGROUND OF INVENTION

[0001] This invention relates to digital dividers, and more particularly to X.5 divide circuits.

[0002] Digital circuits often employ dividers. For example, a clock operating at a higher frequency may be divided by a dividing circuit to generate a lower-frequency clock. Clocked flip-flops can be used when the divisor is a power of two, such as with divide-by-2^N circuits, wherein N is a positive integer.

[0003] Sometimes a divisor is required that is not a power of two, or not even an integer. For example, a 333 MHz clock may be needed, but only a 500 MHz clock is available. The divisor needed is 500/333, or 1.5 (one and a half). Or a 200 MHz clock is needed, requiring a divider circuit with a divisor of 500/200 = 2.5, another non-integer divisor.

[0004] A variety of such divide by X.5 circuits have been devel-

oped, where X is a positive integer (whole number). The duty cycle produced by these circuits may not always be ideal. Sometimes the output clock's duty cycle is altered, such as when a 60%-40% or worse duty cycle is generated.

[0005] What is desired is a divide by X.5 circuit, wherein X is a whole number. A divide by X.5 circuit is desirable that has a near 50%-50% duty cycle.

Brief Description of Drawings

[0006] Figure 1 is an overall block diagram of a divide by 1.5 circuit.

[0007] Figure 2 show the initial PLL with a quadrature VCO in more detail.

[0008] Figure 3 shows the quadrature VCO in more detail.

[0009] Figure 4 shows a divide-by-3 circuit.

[0010] Figure 5 is a diagram of reset-sequencing logic.

[0011] Figure 6 is a diagram of a frequency doubler.

[0012] Figure 7 is a waveform showing operation of the divide by 1.5 circuit.

Detailed Description

[0013] The present invention relates to an improvement in divide by X.5 circuits. The following description is presented to

enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0014] Figure 1 is an overall block diagram of a divide by 1.5 circuit. Phase-locked loop (PLL) 10 includes a quadrature voltage-controlled oscillator (VCO) that outputs four phases of clocks having the same frequency, but being offset in phase from one another by 90-degree increments. The multi-phase clocks from PLL 10 have phases of 0, 90, 180, and 270 degrees.

[0015] Differential pairs of each of the four phases from PLL 10 are converted from differential to single-ended clocks by differential-to-single-ended converters 12. The four phase clocks output by differential-to-single-ended converters 12 are PVCO1, PVCO1B, PVCO3B, and PVCO3, having phases of 0, 180, 270, and 90 degrees, respectively.

[0016] Divide-by-3 circuits 22, 23, 24, 25 are clocked by are PVCO1, PVCO1B, PVCO3B, and PVCO3, respectively, and produce divided-by-3 outputs VDIV3A, VDIV3A#, VDIV3B, VDIV3B#, respectively. The divided-by-3 outputs are one-third the frequency of the input clocks from PLL 10.

[0017] Reset signals RB0, RB2, RB1, RB3 are applied to divide-by-3 circuits 22, 23, 24, 25, respectively. These active-low reset signals are sequenced to periodically reset divide-by-3 circuits 22, 23, 24, 25 after each counts up to three.

[0018] Divided-by-3 outputs VDIV3A, VDIV3A#, VDIV3B, VDIV3B# are applied to the A, A#, B, B# inputs (respectively) of frequency doubler 14. Frequency doubler 14 doubles the frequency of divided-by-3 outputs VDIV3A, VDIV3A#, VDIV3B, VDIV3B# to generate the final output VOUT, which has a frequency that is 1.5 or 3/2 of the frequency output by PLL 10.

[0019] Figure 2 show the initial PLL with a quadrature VCO in more detail. PLL 10 receives a reference clock REFCLK that is divided by M by input divider 52. The high-frequency output signal VCOUT of voltage-controlled oscillator VCO 40 is divided down by feedback divider 58 to a lower feedback frequency. The output signal of divider 58 is ap-

plied to one of the inputs of phase comparator54 to perform phase and frequency comparison with the divided-down reference clock applied to the other input.

[0020] Phase comparator54 controls charge pump 56 to sink or source currents to loop filter 57, which increases or decreases the output voltage VCOIN of loop filter 57. Loop filter 57 is used to filter out high-frequency noise from charge pump56 and to stabilize the closed-loop system of PLL 10.

[0021] The output voltage VCOIN of loop filter 57 is applied as the control voltage to VCO 40 to control its output frequency. This negative feedback system can ensure that the output frequency of the oscillator equals the input clock frequency multiplied by dividing ratio N/M in the locked condition.

[0022] Figure 3 shows the quadrature VCO in more detail. The loop filter's voltage VCOIN is applied to voltage-to-current converter 46. A variable current is generated on line VCTL by voltage-to-current generator 46.

[0023] The bias current on line VCTL is applied to differential stages 41, 42, 43, 44, and controls their propagation delays, such as by varying the current-drive of the differential stages. Thus the propagation delays of differential

stages 41, 42, 43, 44 vary with bias current applied to line VCTL and loop-filter voltage VCOIN.

[0024] Differential stages 41, 42, 43, 44 are connected together in a twisted-ring fashion, since an inversion occurs on the feedback from last differential stage 44 back to first differential stage 41, since the non-inverting (+) output P40 of stage 44 is applied to the inverting input (-) of first differential stage 41. Likewise, the inverting (-) output M40 of stage 44 is applied to the non-inverting input (+) of first differential stage 41. Other stages 41, 42, 43 connect their non-inverting outputs P10, P20, P30 to non-inverting inputs of next stages 42, 43, 44, and inverting outputs M10, M20, M30 to inverting inputs.

[0025] Some of the signals from the current-controlled-delay loop of differential stages 41, 42, 43, 44 in VCO 40 are applied to differential-to-single-ended converters 12. The PLL output VCOUT that is fed back to the feedback inverter in PLL 10 is generated by differential buffer 30, which receives differential signals P40 and M40 from last differential stage 44.

[0026] The first quadrature signal PVCO1 is generated by differential buffer 31, which receives differential signals P10 and M10 from first differential stage 41. This signal

PVCO1 represents the 0 degree relative offset. Since the twisted-ring loop of differential stages 41, 42, 43, 44 has a total of 8 delays in the two passes through the loop, a 90-degree offset occurs after one-quarter of the overall loop delay, or after 2 differential stages. Thus the 90-degree-offset signal, PVCO3 is generated by differential buffer 33 from signals P30, M30 of third differential stage 43. Third differential stage 43 is two stage delays after first differential stage 41.

[0027] The 180-degree signal PVCO1B is generated from first differential stage 41, except that the inputs are reversed. Differential buffer 32 applies the inverted output M10 from first differential stage 41 to its non-inverting (+) input, while the non-inverted output P10 from first differential stage 41 to its inverting (-) input. Similarly, the 270-degfree signal PVCO3B is generated by differential buffer 34 by reversing the inputs from third differential stage 43. Inverted signal M30 from third differential stage 43 is applied to the non-inverting (+) input of differential buffer 34, while the non-inverted output P30 from third differential stage 41 is applied to the inverting (-) input of differential buffer 34.

[0028] Figure 4 shows a divide-by-3 circuit. Divide-by-3 circuit

22 receives a single-ended VCO output signal on its clock CLKIN input. The sequenced active-low reset signal RSB is also received and applied to the reset inputs of flip-flops 61, 62, 63. When RSB is low, flip-flops 61, 62, 63 are cleared and their QB outputs are driven high. NOR gate 74 then drives the divided-by-3 output, CLKOUT low.

[0029] After reset RSB goes high, the states of QB1, QB2, and QB3 are initially 1,1,1. The first rising edge of CLKIN clocks first and second flip-flops 61, 62. The D input to first flip-flop 61 is high, the result of QB1 + QB2', the logic of inverter 66 and NAND gate 72. First flip-flop 61 toggles its QB1 output low, and second flip-flop 62 toggles low, since QB1 is high, producing QB2 low, after the first rising edge of CLKIN.

[0030] The first falling edge of the VCO clock input (CLKIN) clocks third flip-flop 63, which has the previous flip-flop's QB2 (low) as its D input. QB3 of third flip-flop 63 thus goes high after the first falling edge. The high QB3 drives an input to NOR gate 74, which drives CLKOUT low.

[0031] The states of QB1 and QB2 are now 0,0. The second rising edge of CLKIN clocks first and second flip-flops 61, 62. The D input to first flip-flop 61 is high, the result of QB1 + QB2'. First flip-flop 61 keeps its QB1 output low, but

second flip-flop 62 again toggles, with QB2 going high, after the second rising edge of CLKIN.

[0032] The states of QB1 and QB2 are now 0,1. The third rising edge of CLKIN clocks first and second flip-flops 61, 62. The D input to first flip-flop 61 is low, the result of QB1 + QB2'. First flip-flop 61 toggles its QB1 output high, but second flip-flop 62 remains in the same state, with QB2 remaining high, after the third rising edge of CLKIN.

[0033] The states of QB1 and QB2 are now 1,1. This is the same as the initial state after reset. The 3-period cycle now repeats itself. The fourth rising edge of CLKIN clocks first and second flip-flops 61, 62. The D input to first flip-flop 61 is high, the result of QB1 + QB2', the logic of inverter 66 and NAND gate 72. First flip-flop 61 toggles its QB1 output low, and second flip-flop 62 toggles, since QB1 is high, producing QB2 low, after the fourth rising edge of CLKIN, to return to the 0,0 state.

[0034] Third flip-flop 63 delays QB2 from second flip-flop 62 by one-half clock period, since third flip-flop 63 is clocked by inverter 64, which inverts CLKIN. NOR gate 74 OR's QB2 after inverter 68 and QB3, driving CLKOUT high when QB2 is high and QB3 is low. This occurs for one-and-a-half periods of CLKIN, starting with the second

falling edge of CLKIN, and ending with the fourth (first) rising edge of CLKIN.

[0035] Figure 5 is a diagram of reset-sequencing logic. The active-low reset signals to divide-by-3 circuits 22, 23, 24, 25 differ. When the primary reset RSB is de-asserted (goes high), then reset signals RB0, RB1, RB2, and RB3 are each driven high in sequence. Each successive reset is driven high one-half output-clock period after the prior reset is driven high. This causes the divide-by-3 circuits to begin counting at different times, on each edge of the output clock.

[0036] The primary reset RSB is applied to the D input of first flip-flop 75. When its clock, PVCO1, goes high, flip-flop 75 drives its output (Q0) high. AND gate 81 then drives first reset signal RB0 high, since the RB inputs to AND gates 81, 82, 83, 84 have already gone high. First flip-flop 75 continues to drive Q0 and RB0 high on later rising clock edges of PVCO1 since RB remains high. Thus Q0 and RB0 go high and remain high.

[0037] The next rising edge of PVCO3B clocks second flip-flop 76, which receives Q0 from first flip-flop 75 at its D input and drives Q1 high. The high Q1 to AND gate 82 drives RB1 high. The D input to third flip-flop 77 is Q1, so on

the next rising edge of PVCO1B, third flip-flop 77 drives Q2 high, and AND gate 83 drives RB2 high.

[0038] Finally the D input (Q2) to fourth flip-flop 78 is high, so on the next rising edge of PVCO3, fourth flip-flop 78 clocks Q3 high, and AND gate 84 drives RB3 high, allowing the fourth divide-by-3 circuits 25 to begin counting.

[0039] Figure 6 is a diagram of a frequency doubler. Frequency doubler 14 has NAND gate 85 that receives VDIV3A and VDIV3B#, and NAND gate 86 that receives VDIV3B and VDIV3A#. NAND gate 88 sums the outputs of NAND gates 85, 86 to generate the final clock output VOUT.

[0040] VOUT is high when VDIV3B and VDIV3A# are both high, or when VDIV3A and VDIV3B# are both high.

[0041] Figure 7 is a waveform showing operation of the divide by 1.5 circuit. On the Y-axis, PVCO1 and reset RB0 go high, allowing divide-by-3 circuit 22 to begin counting. On the next rising edge of PVCO3B, reset RB1 goes high, allowing divide-by-3 circuit 24 to begin counting. Then on the next rising edge of PVCO1B, reset RB2 goes high, allowing divide-by-3 circuit 23 to begin counting. Finally, on the next rising edge of PVCO3, reset RB3 goes high, allowing divide-by-3 circuit 25 to begin counting. Each divide-by-3 circuits 22, 23, 24, 25 has its reset go high on the

rising edge of its clock input. Since each reset is generated by its corresponding clock, there is no logic hazard.

[0042] The VCO output signals PVCO1, PVCO3, PVCO1B, PVCO3B are free-running with the PLL's oscillator and operate at the input frequency which is divided by 1.5 to get the output frequency of the frequency doubler's output, VOUT. The vertical dashed lines are drawn to correspond to half-clock periods of the final output clock VOUT, but shifted for pipelining delays. Oscillator signals PVCO1, PVCO3, PVCO1B, PVCO3B operate with a period that is 2/3'rds the output period. For 50% duty cycles, one-and-a-half periods of oscillator input PVCO1 equals one output period of VOUT.

[0043] Oscillator signals PVCO1, PVCO3, PVCO1B, PVCO3B are 0, 90, 180, and 270 degrees out of phase with PVCO1, respectively. PVCO1 has a rising edge at the Y-axis, PVCO3 has the next rising edge, then PVCO1B which is an inverse of PVCO1 (180 degrees), and finally PVCO3B rises at 270 degrees.

[0044] The divide-by-3 circuits generate the VDIV3 signals that have a period that is three times the period of the oscillator signal input to the divide-by-3 circuit. For example, PVCO1 is input to first divide-by-3 circuit 22, which gen-

erates VDIV3A. PVCO1 has a rising edge at the Y-axis, another in the second period of VOUT, a third rising edge in the third period of VOUT, and the fourth rising edge (ending the third full period of PVCO1) at the end of the fourth period of VOUT, when VDIV3A falls, ending its first period. VDIV3A rises mid-way in its period for a 50-50 duty cycle. VOUT doesn't start pulsing until several periods after reset ends.

[0045] The next divide-by-3 circuit 24 is activated by RB1 going high at the end of the first period of VOUT. This divide-by-3 circuit 24 is clocked by PVCO3B, which is the 270-degee oscillator signal. VDIV3B is generated by divide-by-3 circuit 24 and is driven high on the second falling edge of PVCO3B after reset RB1 ends.

[0046] Each of the four divide-by-3 circuits 22, 23, 24, 25 drives its output high on the second rising VCO-clock edge after its corresponding reset goes high. At the Y-axis, RB0 goes high, activating divide-by-3 circuit 22 to begin counting with PVCO1, and driving VDIV3A high at the second falling edge of PVCO1. One-and-a-half periods of PVCO1 later, VDIV3A goes low. Then VDIV3A goes high after another one-and-a-half periods of PVCO1. This continues, producing a 50%-50% duty cycle of VDIV3A.

[0047] RB1 then goes high, activating divide-by-3 circuit 24 to begin counting with PVCO3B, and driving VDIV3B high at the second falling edge of PVCO3B. One-and-a-half periods of PVCO3B later, VDIV3B goes low. Then VDIV3B goes high after another one-and-a-half periods of PVCO3B. This continues, producing a 50%-50% duty cycle of VDIV3B.

[0048] When RB2 goes high, divide-by-3 circuit 23 begins counting with PVCO1B, and driving VDIV3A# high at the second falling edge of PVCO1B. One-and-a-half periods of PVCO1B later, VDIV3A# goes low. Then VDIV3A# goes high after another one-and-a-half periods of PVCO1B. This continues, producing a 50%-50% duty cycle of VDIV3A#.

[0049] Finally, when RB3 goes high, divide-by-3 circuit 25 begins counting with PVCO3, and driving VDIV3B# high at the second falling edge of PVCO3. One-and-a-half periods of PVCO3 later, VDIV3B# goes low. Then VDIV3B# goes high after another one-and-a-half periods of PVCO3. This continues, producing a 50%-50% duty cycle of VDIV3B#.

[0050] ALTERNATE EMBODIMENTS

[0051] Several other embodiments are contemplated by the inventors. Other divisors can be achieved by substituting a

divide-by-Y circuit for the divide-by-3 circuits of Fig. 1, where Y is another odd integer (5, 7, 9, ...). For example, a divide by 2.5 circuit uses divide-by-5 circuits rather than divide-by-3 circuits, while a divide by 3.5 circuit uses divide-by-7 circuits rather than divide-by-3 circuits. Phase offsets may not be exactly 90, 180, 270 degrees but may vary somewhat.

[0052] Differential buffers and stages can be implemented in a variety of ways, such as by using current-mirrored differential amplifiers, sense amplifiers, etc. AND gates can be implemented as a NAND gate driving an inverter, and other logic adjustments can be made.

[0053] The abstract of the disclosure is provided to comply with the rules requiring an abstract, which will allow a searcher to quickly ascertain the subject matter of the technical disclosure of any patent issued from this disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. 37 C.F.R. §1.72(b). Any advantages and benefits described may not apply to all embodiments of the invention. When the word "means" is recited in a claim element, Applicant intends for the claim element to fall under 35 USC § 112, paragraph 6. Often a label of one or more words precedes

the word "means". The word or words preceding the word "means" is a label intended to ease referencing of claims elements and is not intended to convey a structural limitation. Such means-plus-function claims are intended to cover not only the structures described herein for performing the function and their structural equivalents, but also equivalent structures. For example, although a nail and a screw have different structures, they are equivalent structures since they both perform the function of fastening. Claims that do not use the word means are not intended to fall under 35 USC § 112, paragraph 6. Signals are typically electronic signals, but may be optical signals such as can be carried over a fiber optic line.

[0054] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.